VLSI DESIGN & VERIFICATION
Course Code: 16CS322

Module 1
Introduction
Introduction to Digital VLSI Design Flow, High Level Design Representation, Transformations for High Level Synthesis.

Module 2
Scheduling, Allocation and Binding: Introduction to HLS(High Level Synthesis): Scheduling, Allocation and Binding Problem, Scheduling Algorithms, Binding and Allocation Algorithms.

Module 3
Logic Optimisation and Synthesis: Two level Boolean Logic Synthesis, Heuristic Minimisation of Two-Level Circuits, Finite State Machine Synthesis, and Multilevel Implementation.

Module 4
Verification: Binary Decision Diagram: Binary Decision Diagram: Introduction and construction, Ordered Binary Decision Diagram, Operations on Ordered Binary Decision Diagram.

Module 5
Temporal Logic and Introduction to Digital Testing: Introduction and Basic Operations on Temporal Logic, Syntax and Semantics of CLT, Equivalence between CTL Formulas , Introduction to Digital VLSI testing.